

**ABSTRACT OF THE DISCLOSURE**

This invention is intended to improve reliability of a nonvolatile semiconductor memory device and reduces a memory cell size of the nonvolatile semiconductor memory device. A  
5 memory cell which includes source/drain diffusion layers in a p-type well formed in a silicon substrate, silicon nitride dots which are located between silicon oxide films and into which charges are injected, a control gate 212, and assist gates is formed. Programming is conducted to the memory cell by  
10 injecting electrons into the drain-side silicon nitride dots or the source-side silicon nitride dots. Since silicon nitride serving as a charge injected section is in the form of dots, it is possible to suppress movement of the charges in a channel direction, to prevent the charges on a source end portion and  
15 those on a drain end portion from being mixed together, and to improve charge holding characteristic of the memory cell. Even in the case where a gate length is shortened, the charge holding characteristic can be secured.